CLAIMS

What is claimed is:

1	1. A printed circuit board (PCB) comprising:
2	a first signal routing layer formed on a first surface of the PCB;
3	at least one conductive plane and/or a second signal routing layer;
4	at least one padless via extending from the first signal routing layer to the at
5	least one conductive plane and/or the second signal routing layer, the at least one
6	padless via in electrical contact with the at least one conductive plane and/or a
7	conductive trace on the second signal routing layer; and
8	a layer of solder mask material formed over the first signal routing layer, the
9	layer of solder mask material having at least one opening to expose the at least one
10	padless via.

- 1 2. The PCB of claim 1, wherein the second signal routing layer is an inner signal
- 2 routing layer and the at least one padless via is a blind padless via extending from the
- 3 first signal routing layer to the second signal routing layer.
- 1 3. The PCB of claim 1, further comprising a via plug formed within the padless
- 2 via.
- 1 4. The PCB of claim 3, wherein the via plug is formed of an electrically
- 2 conductive material.
- 1 5. The PCB of claim 1, further comprising a component attached to the PCB with
- 2 a solder interconnection between a contact pad on a bottom surface of the component
- 3 and the at least one padless via.

- 1 6. A printed circuit board (PCB) comprising:
- a first signal routing layer formed on a first surface of the PCB;
- at least one conductive plane and/or a second signal routing layer; and
- an array of interconnections formed on the first surface of the PCB, the array of
- 5 interconnections comprises at least one padless via extending from the first signal
- 6 routing layer to the at least one conductive plane and/or the second signal routing layer,
- 7 wherein the padless via is in electrical contact with the at least one conductive plane
- 8 and/or a conductive trace on the second signal routing layer.
- 1 7. The PCB of claim 6, further comprising an electrically conductive via plug
- 2 formed within the at least one padless via.
- 1 8. The PCB of claim 6, wherein the array of interconnections further comprises at
- 2 least one contact pad electrically coupled with a conductive trace on the first signal
- 3 routing layer, wherein the at least one contact pad has a diameter less than 18 mils.
- 1 9. The PCB of claim 6, further comprising at least two conductive traces formed
- 2 on the first signal routing layer between the at least one padless via and an adjacent
- 3 interconnection.
- 1 10. The PCB of claim 9, wherein the array of interconnections has an array pitch of
- 2 0.8 mm or less.
- 1 11. The PCB of claim 10, wherein the at least two conductive traces have a width of
- 2 approximately 3 mils.

- 1 12. The PCB of claim 6, wherein the at least one padless via has a diameter of 12
- 2 mils or less.

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- 13. A system comprising:
- 2 a printed circuit board (PCB) comprising a first signal routing layer formed on a
- 3 first surface of the PCB, at least one conductive plane and/or a second signal routing
- 4 layer, and an array of interconnections formed on the first surface of the PCB, wherein
- 5 the array of interconnections comprises at least one padless via extending from the first
- 6 signal routing layer to the at least one conductive plane and/or the second signal routing
- 7 layer, the at least one padless via electrically connected to the at least one conductive
- 8 plane and/or a conductive trace on the second signal routing layer; and
- a component attached to the PCB by a plurality of solder ball interconnections
- between the array of interconnections formed on the first surface of the PCB and a
- 11 corresponding array of contact pads disposed on a bottom surface of the electronic
- 12 component.
- 1 14. The system of claim 13, wherein the component is a ball grid array (BGA)
- 2 component having an array pitch less than 1.0 mm.
- 1 15. The system of claim 14, further comprising at least two conductive traces on the
- 2 first signal routing layer routed between the at least one padless via and an adjacent
- 3 interconnection.
- 1 16. The system of claim 15, wherein a width of the at least two conductive traces is
- 2 approximately 3 mils.

- 1 17. The system of claim 13, wherein the at least one padless via has a diameter of
- 2 12 mils or less.
- 1 18. The system of claim 13, wherein the PCB is a motherboard and the component
- 2 is a processor.
- 1 19. A method of fabricating a printed circuit board (PCB) comprising:
- 2 forming a first signal routing layer on a first surface of a printed circuit board
- 3 (PCB); and
- forming an array of interconnections on the first surface of the PCB, the array of
- 5 interconnections comprising at least one padless via extending from the first signal
- 6 routing layer to a conductive plane and/or a second signal routing layer, wherein the
- 7 first padless via is in electrical contact with the conductive plane and/or a conductive
- 8 trace on the second signal routing layer.
- 1 20. The method of claim 19, wherein the second signal routing layer is an inner
- 2 signal routing layer and the at least one padless via is a blind via extending from the
- 3 first signal routing layer to the second signal routing layer.
- 1 21. The method of claim 19, wherein forming an array of interconnections on the
- 2 first surface of the PCB comprises forming an array of interconnections having an array
- 3 pitch of 0.8 mm or less.
- 1 22. The method of claim 21, further comprising routing at least two conductive
- 2 traces on the first signal routing layer between the at least one padless via and an
- 3 adjacent interconnection.

- 1 23. The method of claim 19, further comprising forming a via plug within the at
- 2 least one padless via.
- 1 24. The method of claim 19, wherein forming a via plug within the at least one
- 2 padless via comprises overplating the at least one padless via to form a via plug of
- 3 plating material.
- 1 25. The method of claim 19, wherein forming an array of interconnections on the
- 2 first surface of the PCB comprises forming at least one contact pad on the first surface
- 3 of the PCB adjacent to the at least one padless via, the at least one contact pad in
- 4 electrical contact with a conductive trace on the first signal routing layer.
- 1 26. A method of attaching a component to a printed circuit board (PCB)
- 2 comprising:
- aligning solder balls attached to an array of contact pads on a bottom surface of
- 4 the component with a corresponding array of interconnections formed on a first surface
- 5 of the PCB, the array of interconnections comprising at least one padless via extending
- 6 from a first signal routing layer on the first surface of the PCB to a conductive plane
- 7 and/or a second signal routing layer within the PCB, wherein the at least one padless
- 8 via is in electrical contact with the conductive plane and/or a conductive trace on the
- 9 second signal routing layer; and
- reflowing the solder balls to electrically connect the array of contact pads to the
- 11 corresponding array of interconnections.

- 1 27. The method of claim 26, wherein the solder balls comprise a solder shell
- 2 surrounding a solid center of a material having a higher melting temperature than the
- 3 solder shell.
- 1 28. The method of claim 27, wherein the solder shell is made of a lead-free solder
- 2 and the solid center is copper or aluminum.
- 1 29. The method of claim 26, wherein the component is an electronic component
- 2 housed in a ball grid array (BGA) package having a BGA pitch of 0.8 mm or less.
- 1 30. The method of claim 29, wherein the component is a land grid array (LGA)
- 2 socket.